REMARKS

After the foregoing amendment, claims 1-6 and 14-16 are active in the present application. Claims 7-13 have been cancelled and new claims 14-16 have been added. In addition, claim 2 has been amended. Reconsideration and allowance of the application, as amended, are respectfully requested.

The present invention is directed to a RTP packet handler that includes a CPU and a protocol processor. The normal OS and protocol stack software executes on the CPU and a RTP packet handler module for processing RTP packets executes on the protocol processor. In this way, RTP packet processing is off-loaded from the CPU, which frees up the CPU to execute other tasks while the protocol processor handles RTP packets, and additionally accelerates RTP packet processing.

Previously presented method claims 7-13 have been cancelled because they did not clearly distinguish the steps performed by a CPU and those by a separate, protocol processor.

Claim 2 has been amended to recite that the protocol processor is a RISC processor. New claim 15, which depends from claim 6, also recites that the protocol processor is a RISC processor. The amendment to claim 2 and new claim 15 are supported in the specification at page 3, lines 26-27.

New claims 14 and 16, which depend from different base claims, both recite that the protocol processor includes a

dual port memory that is used for communicating with the central processor. New claims 14 and 16 are supported in the specification at page 3, lines 31-33 and FIG. 6.

Thus, no new matter has been added by the amendments.

Claims 1-9 were under 35 USC 102(3) as anticipated by US Patent No. 6,480,892 (Levay). Applicants respectfully traverse the rejection.

Levay discloses a test apparatus 12 including a pair of LAN cards 20, 22 and a packet filter 24 (Levay FIG. 1 and col. 2, lines 61-67). The test apparatus 12 monitors network traffic between hosts 14 and 16 and selectively discards incoming packets in order to cause packet loss into the data flow and thereby test media software operating on the hosts 14 and 16. (Levay at col. 2, lines 57-60). The LAN cards 20 and 22 allow the test apparatus 12 to transmit and receive data packets. The packet filter 24 receives incoming data packets and based on some predetermined rules selectively discards some of the incoming packets and generates a reduced set of packets that is transmitted over the network to the hosts (Levay at col. 3, lines 1-7).

The test apparatus 12 is implemented using a conventional computer workstation running an OS. The protocol stack for monitoring the network and the packet filter 24 are implemented in software stored in a memory. (Levay, col. 3, lines 25-29).

The present invention, as discussed above and defined in independent claim 1 and 5, includes a CPU upon which an

OS executes and a separate, protocol processor that executes a RTP packet handler module. Thus, the present invention differs from conventional systems because of the addition of a separate processor for handling RTP packets. The protocol processor may be a RISC processor (amended claim 2) and the RTP packet handler module may be either a software routine or a microcode routine (claim 4).

Since Levay does not disclose both a CPU and a protocol processor that processes RTP packets, claims 1-9 are not anticipated by Levay. Accordingly, Applicants respectfully request reconsideration and withdrawl of the rejection of claims 1-6 as anticipated by Levay.

New claim 14 depends from claim 2 and recites that the protocol processor includes a dual port memory. Claim 14 is not anticipated by Levay for the same reasons as discussed above, namely, that Levay does not disclose two separate processors, a CPU and a protocol processor.

New claims 15 and 16 depend (indirectly) from independent claim 5 and respectively recite that the protocol processor is a RISC processor and includes a dual port memory. Neither of these claims is anticipated by Levay because Levay does not disclose a protocol processor that is a separate, RISC processor with a dual port memory.

> Accordingly, claims 15-16 are believed to be in condition for allowance.

1.0

In view of the foregoing amendments and remarks, it is respectfully submitted that the present application,

including claims 1-6 and 14-16, is in condition for allowance and such action is respectfully requested.

Respectfully submitted,

Man Kuk Lo et al.

BY:

Charles E. Bergere

Reg. No. 36,337

FREESCALE SEMICONDUCTOR, INC.

Customer No. 23125

and the first of the second of